

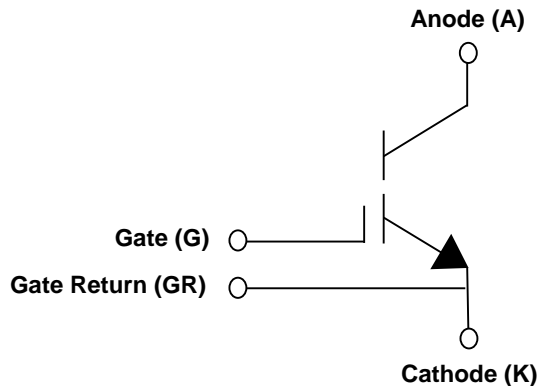
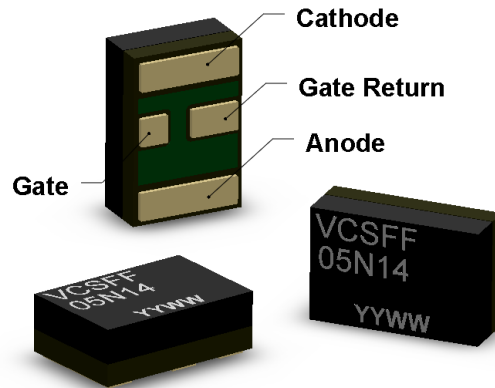
The **VCSFF05N14A11** (Branded VCSFF05N14) replaces the **VCSFF05N14A10**.

The **VCSFF05N14A11** is a MOS-Controlled Thyristor (MCT) packaged in the F-Pak SMT package. It features high peak current capability and a low on-state voltage drop. Additionally, it demonstrates extremely high turn-on di/dt capability and virtually no turn-on delay jitter making it ideally suited for a wide variety of capacitor discharge applications requiring precise timing and rapid energy transfer capability.

The **F-Pak** is a custom surface mount package in which the semiconductor is “flip-chip” mounted onto a high temperature PCB substrate then encapsulated in epoxy. It offers a small footprint and low inductance interface that allows for installation using conventional automated handling equipment. See handling and storage notes presented later in this document.

## KEY PRODUCT FEATURES

- 1400V Repetitive Peak Off-State Voltage
- $V_{GK} = 0V = OFF$
- 120kA/ $\mu$ Sec di/dt Capability
- < 100nSec Turn-On Delay Time
- 3kA Repetitive Anode Current



## MAXIMUM RATINGS

	SYMBOL	VALUE	UNITS
Repetitive Peak Off-State Voltage	$V_{DRM}$	1400	V
Repetitive Peak Reverse Voltage	$V_{RRM}$	-5	V
Off-State Rate of Change of Voltage Immunity ( $V_D=1400V$ )	dv/dt	5000	V/ $\mu$ Sec
Non-repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	$I_{TSM}$	4800	A
Repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	$I_{TRM}$	3000	A
Rate of Change of Current	di/dt	120	kA/ $\mu$ Sec
Continuous Gate-Cathode Voltage	$V_{GKS}$	+/-20	V
Peak Gate-Cathode Voltage	$V_{GKM}$	+/-25	V
Required Off-State Gate-Cathode Voltage	$V_{GDM}$	0	V
Maximum Junction Temperature	$T_{JM}$	125	$^{\circ}C$
Maximum Soldering Temperature (Installation)		220	$^{\circ}C$

## ELECTRICAL CHARACTERISTICS

$T_C=25^\circ\text{C}$  unless otherwise specified

Parameters	Symbol	Test Conditions	Measurements			
			Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	$V_{D(BR)}$	$V_{GK}=0\text{V}, I_D=250\mu\text{A}$	1400			V
Anode-Cathode Off-State Current	$I_D$	$V_{GK}=0\text{V}, V_D=1550\text{V}$	$T_C=25^\circ\text{C}$		500	nA
			$T_C=50^\circ\text{C}$		1	$\mu\text{A}$
			$T_C=125^\circ\text{C}$		5	$\mu\text{A}$
Gate-Cathode Leakage Current	$I_{GM}$	$V_{GK}= \pm 15\text{V}$		4	10	nA
Gate-Cathode Turn-On Threshold Voltage	$V_{GK(TH)}$	$V_{AK}=12\text{V}, I_D=1\text{mA}$		.8		V
Input Capacitance	$C_{ISS}$	Bias=6V, Freq.=120Hz		1.55		nF
Turn-on Delay Time	$t_{d(ON)}$	0.15 $\mu\text{F}$ Capacitor Discharge $T_J=25^\circ\text{C}, V_{GK}=0\text{V to }+10\text{V}$		60	100	nSec
Rate of Change of Current	$di/dt$	$V_{DD}=1000\text{V}, R_G=3.0\Omega, L_S=10\text{nH},$ $R_{SENSE}=0.010\Omega$ See Figures 1 & 2.		85		$\text{kA}/\mu\text{Sec}$
Peak Anode Current	$I_{DM}$	See Figures 1 & 2.		3000		A
Turn-on Delay Time	$t_{d(ON)}$	0.16 $\mu\text{F}$ Capacitor Discharge $T_J=25^\circ\text{C}, V_{GK}=0\text{V to }+10\text{V}$		40		nSec
Rate of Change of Current	$di/dt$	$V_{DD}=1200\text{V}, R_G=3.0\Omega, L_S=8\text{nH},$ $R_{SENSE}=0.010\Omega$ See Figures 1 & 2.		120		$\text{kA}/\mu\text{Sec}$
Peak Anode Current	$I_{DM}$	See Figures 1 & 2.		4000		A

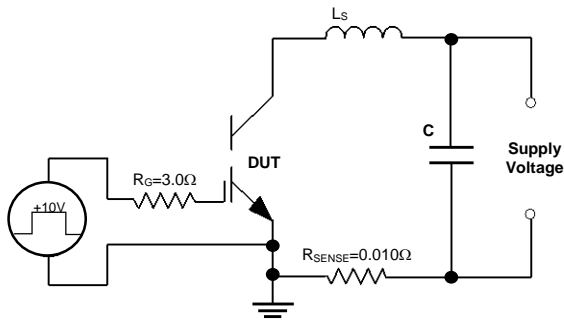


Figure 1. 0.16 $\mu\text{F}$  Capacitor Discharge Circuit

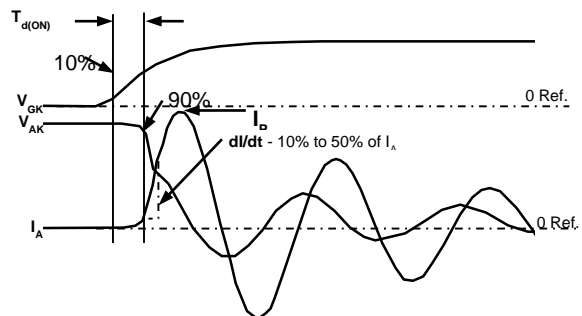
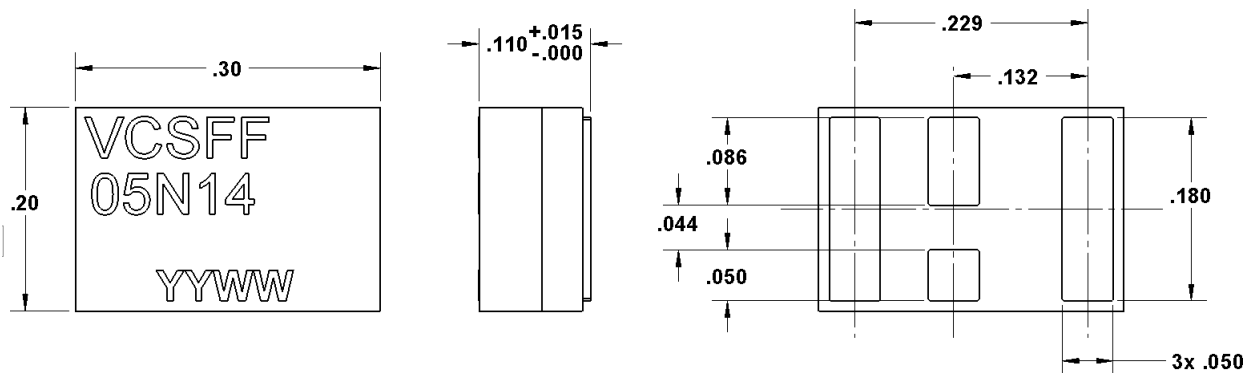


Figure 2. 0.16 $\mu\text{F}$  Capacitor Discharge Waveforms



### DATE CODE

YY = LAST 2 DIGITS OF CALENDAR YEAR  
WW = WORK WEEK OF THE CALENDAR YEAR

### DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED:  
TWO PLACE DECIMAL  $\pm 0.010$  THREE PLACE DECIMAL  $\pm 0.004$

Figure 3. Critical Package Dimensions and Markings

## HANDLING AND STORAGE

### ESD Sensitivity



**THIS DEVICE IS ESD SENSITIVE.** OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS (REF. JESD625).

**IMPROPER HANDLING OF THIS DEVICE MAY PERMANENTLY DAMAGE THE DEVICE AND RENDER IT UNUSABLE.**

### Moisture Sensitivity

F-Pak SMD Packages are qualified as **MSL Level 3 maximum SMD solder reflow temperature of 220°C.**

In accordance with **IPC/JEDEC J-STD-033C**, F-Pak products are dry-baked then packed in a Moisture Barrier Bag (MBB) containing desiccant and a Humidity Indicator Card (HIC). When the Moisture Barrier Bag is opened or compromised refer to **IPC/JEDEC J-STD-033C** for proper HIC interpretation, dry baking, floor life and storage procedures.

### Solderability

It has been determined that the component pads of the F-Pak are **CONSISTENTLY MILDLY OXIDIZED** as a result of the manufacturing and required dry-baking processes (Ref. J-STD-033, MSL Level 3, Table 4-2). Customers should be aware that solderability testing of finished dry-baked product indicates that the amount of oxidation present is such that it **MAY REQUIRE THE USE OF MODERATE OR HIGHLY ACTIVE FLUX** to achieve satisfactory solder wetting. Customers should first qualify this product with their specific SMD storage, baking and reflow processes/materials to ensure satisfactory solderability is achievable.

**CAUTION:** Additional baking of F-Pak SMD packages may cause increased oxidation and/or intermetallic growth of the terminations, which if excessive, can result in solderability problems during board assembly. The temperature and time for baking this SMD package should, therefore, be limited with solderability considerations in mind.

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